their gates connected to word line WL1. The other two FET transistors T2 and T4 have their gates connected to word line WL2. The transistors T1 and T2 have their drains connected to bit line BL1; and transistors T3 and T4 have their drains connected to bit line BL2. Transistors T1, T2, T3 and T4 have their sources connected together in a common reference potential.

Summary

Advantages of this invention include as follows:

1) Double channels are provided for each cell.

2) There are common sources so there is as follows:

a) No need of a virtual ground technique.

b) No need of decoding source lines.

While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with modifications within the spirit and scope of the appended claims, i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the claims which follow.

Having thus described the invention, what is claimed as new and desirable to be secured by Letters Patent is as follows:

1. A method of manufacture of a semiconductor device on a P– silicon semiconductor substrate having a surface comprising

a) forming an N+ source region layer on the surface of said semiconductor substrate, said N+ source layer having an exposed surface,

b) forming a dielectric layer on the surface of said source region layer,

c) patterning and etching said dielectric layer forming a first dielectric layer pattern with openings therein down to said exposed surface of said N+ source layer,

d) forming a silicon epitaxial channel layer in said openings in said first dielectric layer pattern, said silicon epitaxial channel layer having exposed surfaces and doping said epitaxial layer with a P– dopant,

e) forming an N+ drain layer on the surface of said silicon epitaxial layer to form drain regions over the remainder of said silicon epitaxial layer by doping with an N+ dopant,

f) removing said dielectic layer and then forming a second dielectric layer on the surface of said device including said N+ drain layer,

g) forming and patterning a conductor layer containing silicon over said second dielectric layer,

h) forming an N+ implant mask with an N+ opening over a region of said epitaxial channel layer and ion implanting through said N+ opening in said implant mask into said region,

i) forming a code implant mask over said conductor layer, and

j) ion implanting through said code implant mask into the device.

2. The method of claim **1** wherein said conductor layer comprises a material selected from the group consisting of polysilicon and a polycide selected from the group consisting of WSi_2, $TiSi_2$, $CoSi_2$, $MoSi_2$, and $TaSi_2$.

3. The method of claim **1** wherein said ion implanting through said code implant mask into the device employs a dose of boron.

4. The method of claim **3** wherein said dose comprises boron ions implanted within the range from about 1E13 cm^{-2} to about 5E14 cm^{-2}.

5. The method of claim **4** wherein forming an N+ source layer on the surface of said semiconductor substrate is performed by an arsenic ion implant.

6. The method of claim **4** wherein said dose is applied at from about 100 keV to about 200 keV.

7. The method of claim **6** wherein forming an N+ drain layer on the surface of said silicon epitaxial layer is performed by ion implant of an N– dopant.

8. The method of claim **4** wherein forming an N+ drain layer on the surface of said silicon dielectric layer is formed by ion implanting of an N– dopant.

9. The method of claim **4** wherein forming an N+ drain layer on the surface of said silicon epitaxial layer is performed by thermal deposition from a source of a dopant selected from the group consisting of of arsenic and phosphorous and antimony into said silicon dielectric layer and annealing.

10. The method of claim **4** wherein forming an N+ source layer on the surface of said semiconductor substrate is performed by an arsenic ion implant.

11. The method of claim **5** wherein forming an N+ drain layer on the surface of said silicon epitaxial layer is performed by ion implant of an N– dopant.

12. The method of claim **6** wherein forming an N+ drain layer on the surface of said silicon epitaxial layer is performed by thermal deposition and diffusion of a material selected from arsenic, phosphorus and antimony.

13. The method of claim **6** wherein forming an N+ source layer on the surface of said semiconductor substrate is performed by an arsenic ion implant.

14. A method of manufacture of a semiconductor device on a P– silicon semiconductor substrate having a surface comprising

a) forming an N+ source region layer on the surface of said semiconductor substrate, said N+ source layer having an exposed surface,

b) forming a dielectric layer on the surface of said source region layer,

c) patterning and etching said dielectric layer forming a, first dielectric layer pattern with openings therein down to said exposed surface of said N+ source region layer,

d) forming a silicon epitaxial channel layer in said openings in said first dielectric layer pattern, said silicon epitaxial channel layer having exposed surfaces and being doped with a P– dopant,

e) forming an N+ drain layer on the surface of said silicon epitaxial layer to form drain regions over the remainder of said silicon epitaxial layer by doping with an N+ dopant,

f) removing said dielectric layer and then forming a second dielectric layer on the surface of said device including said N+ drain layer,

g) forming and patterning a conductor layer containing silicon over said second dielectric layer,

h) forming an N+ opening over a region of said epitaxial channel layer and ion implanting through said N+ opening in said implant mask into said region,

i) forming a code implant mask over said conductor layer, and

j) ion implanting through said code implant mask into the device.

15. The method of claim **14** wherein said conductor layer comprises a material selected from the group consisting of